



Luxembourg, 20 June 2023

Environmental and Social Completion Sheet (ESCS)¹

Overview

Project Name: MENTA (EGF VD)

Project Number: 2021-0122

Country: France

Project Description: Menta is a French designer of Embedded Field-Programmable Gate Arrays ("eFPGA"). FPGAs are microchips that sit between ASICs (Application-Specific Integrated Circuits) and regular CPUs that provide a more efficient and flexible circuit design. Menta's design allows the embedding of such an FPGA chip design into an ASIC or CPU directly. The Company only sells intellectual property, it does not manufacture the chips itself.

Summary of Environmental and Social Assessment at Completion

EIB notes the following Environmental and Social performance and key outcomes at Project Completion.

The financed activities do not fall under the EU Directive 2014/52/EU amending the EIA Directive 2011/92/EU and were not subject to the Environmental Impact Assessment. The project's activities and investments have been carried out in the existing facilities and due to the project's R&D character, the direct environmental impact of the financed activities is negligible.

The eFPGA products and solutions developed by the project offer significantly lower power consumption compared to standard FPGA technologies and enable a variety of new applications, e.g. in the area of edge computing and the Internet of Things (IoT), allowing for field devices to be re-programmed and adapted to changing environments. Unlike the design process for standalone FPGAs, embedded FPGA designers can select the exact amount of logic, data storage facility, and memory resources required for their customers' applications, making it more cost effective and sustainable than existing FPGA solutions.

Summary opinion of Environmental and Social aspects at completion:

EIB is of the opinion based on reports from the promoter, site visits by the EIB team, that the Project has been implemented in line with EIB Environmental and Social Standards, applicable at the time of appraisal.

¹ The template is for ILs and FLs